## NEC Provides Design Tool to Faraday Technology Corporation in Taiwan

- Synthesizing Low Delay and Low Latency Circuits -

**Tokyo, January 19, 2017 -** <u>NEC Corporation</u> (NEC; TSE: 6701) today announced that it provided Faraday Technology Corporation, a major fabless IC vendor in Taiwan, with CyberWorkBench®, a design tool capable of synthesizing Application Specific Integrated Circuit (ASIC)/Field Programmable Gate Array (FPGA) circuits from the C programming language.

Faraday is utilizing CyberWorkBench (CWB) to design FPGA for communication control. The FPGA are designed as an ASIC prototype for communication control, with the scope of the product's application scheduled to be extended to ASIC. Sales of CWB to Faraday were conducted by NEC's partner, Avant Technology Inc.

CWB is an integrated design environment consisting of a high-level synthesis tool, as well as dynamic and static verification capabilities that shorten the design period by automatically converting the Large Scale Integrated Circuit (LSI) functions written in C language into circuits that satisfy both the circuit size (area) and performance needs. CWB has been used for design control LSI for equipment that requires high reliability such as satellites, communications equipment and backbone servers. Since its launch in 2006, CWB has been introduced internationally to more than 100 companies in the manufacturing industry.

The physical communication layer is required to have low delay (high frequency) and low latency (short operation cycle) circuits. Due to the complex functions, including error correction, it is not easy even for an experienced Register Transfer Level (RTL) designer to design a circuit that meets these two strict conditions. This product offers a variety of synthesizing options to synthesize low delay and low latency circuits from the functions written in C language. The use of these options facilitates Faraday to synthesize a circuit that satisfies the low delay and low latency specifications in the physical layer of high-performance communications equipment.

The function to be implemented in the circuit is written in C language in the initial design phase. When designing a low latency circuit, it is necessary to change the function written in C language into the implement high-performance contents that processing. In conventional manual RTL design, these changes require a great deal of fixing work and pose difficulties in terms of preventing errors from occurring. As the use of this product facilitates Faraday to automatically reflect the changes made in the functions written in C language in the circuits, the company is now able to reduce the manual hours for design to one sixth and to help prevent errors from occurring.

"NEC has been focusing on the Solutions for Society business, and it will contribute to the enhancement of corporate competitiveness by leveraging its experience in providing CWB to Faraday and by increasing the sales of the product to the diverse manufacturers involved in LSI design," said Aritomo Ishikawa, General Manager, Embedded Business Sales Division, NEC Corporation.

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