OFDM Baseband Processor by Noesis Technologies

July 21, 2014 – Noesis Technologies announced today the immediate availability of its ntOFDM_BBP custom baseband processor, which implements the physical layer of an OFDM, time division du-plexing (TDD) system. The baseband processor includes both transmission and reception bit-level and symbol-level processing chains including a sophisticated synchronization unit. The host interface is based on SPI protocol as well as with handshaking/interrupt ports. This custom system implements a subset of 802.16d standard functional options/features and is highly configurable via the integrated register file. An RF interface module is also included, compatible with Analog Devices AD9361 RF transceiver.
The Bit-level processing block (BLPB) transmission chain implements the following functional units : randomization, FEC encoding, interleaving and symbol mapping. In BLPB reception chain the following operations are implemented: soft symbol demapping, deinterleaving, FEC decoding and derandomization. The FEC module is based on the implementation of the Reed Solomon algorithm.
The Symbol-level processing block (SLPB) transmission chain implements the following functional units: OFDM symbol transmitter, IFFT , CP insertion. In reception chain the SLPB module is preceded by the synchronization unit, which is searching for known preamble values in order to locate the start an incoming wimax sub-frame. Once the sub-frame is located, frequency offset compensation is applied and received information is propagated down to SLPB reception chain. In SLPB reception chain the following operations take place: CP removal, FFT, OFDM symbol receiver, channel estimation, phase off-set compensation and channel equalization.

Applications

The ntOFDM_BBP core implements a custom, OFDM, TDD based base-band processor which can be used in a variety of wireless broadband applications. The core can be delivered as RTL source code, FPGA or ASIC (GDSII) netlist, under an End-User License Agreement.

About Noesis Technologies P.C.

Noesis Technologies, P.C. is a silicon IP provider specialized in hardware implementation of high computational complexity telecom algorithms. Our hardware accelerator IP solutions allow telecom system developers to significantly off load demanding tasks from the CPU and to drastically decrease execution time thus boosting the overall system performance. Our IP cores present an industry leading combination of high performance, low power and low die-area, as well as easy customization for adaptability to a wide range of applications. Noesis offers a complete portfolio of Forward Error Correction IP core solutions that includes Reed Solomon Codecs, Viterbi Decoders, Turbo Product and Turbo Convolutional Codecs, BCH codecs, (De)Interleavers, Channel Emulators. The company additionally offers a range of cores in the areas of security, networking, audio/voice compression and telecom DSP. Our solutions have been integrated in our customers' end-products in telecom, aerospace and defense systems. Noesis Technologies is headquartered at Patras Science Park, GR 26504 Patras, Greece and has offices at San Jose, CA 95134, USA.

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