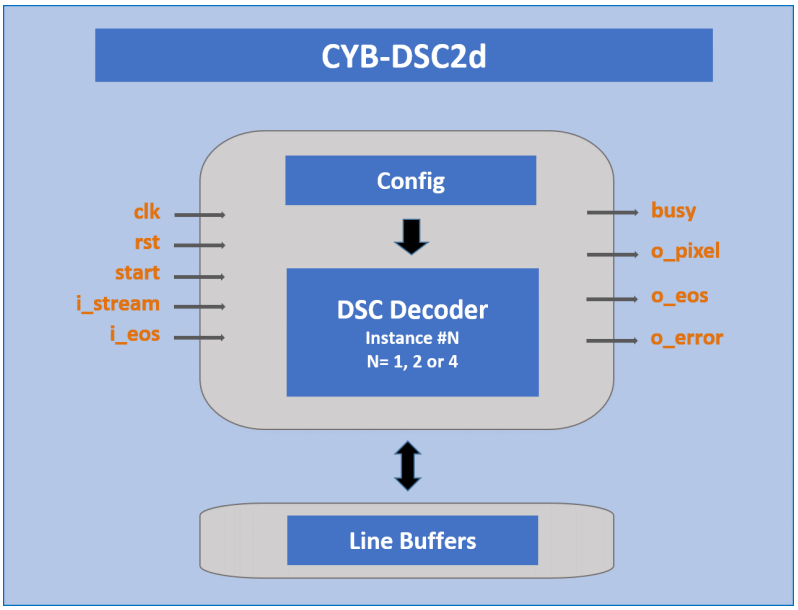
Overview of DSC Decoder IP



Display Stream Compression (DSC) standard was announced by Video Electronics Standards Association (VESA) in 2014 for video data compression and has been also adopted into the VESA's eDP v1.4 and the MIPI DSI standard.

Compliant with the VESA DSC 1.2a and 1.2b standards, CYB-DSC2d IP core supports various coding schemes (MMAP, BP, MPP, ICH) as well as color formats in YCbCr 4:4:4, 4:2:2, 4:2:0 and RGB. It performs visually lossless compression, low gate count and latency for ultra-high definition display applications. It can be fastly and easily integrated into ASIC and FPGA applications for 4K / UHD TV, DisplayPort 1.4, USB Type-C device and AR / VR product.

Feature

- Compliant with the VESA DSC 1.2a and 1.2b standards
- Perform decoding
- Support MMAP, BP, MPP and ICH
- Support 4:4:4, 4:2:2, 4:2:0 and RGB
- Support 8/10/12 bits per component
- Support 3 pixels per clock
- Configurable features for gate count, speed or power requirement
- Programmable display resolutions

Deliverable

- Flexible licensing
- Documentation
- Netlist
- Verilog or VHDL
- Technical support

Application

- 4K / UHD / Digital TV
- Automotive Video
- USB Type-C device
- AR / VR product