

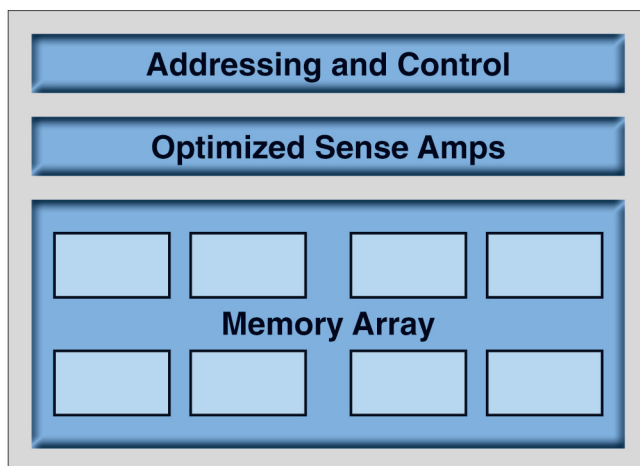
Novelics coolREG™

coolREG memory IPs provide solutions for synchronous single-port, dual-port, and two-port register files requirements. The coolREG IP is based on the production-proven, foundry-provided 6T SRAM (single-port) or 8T SRAM (dual- or two-port) cell and offers advanced leakage control features and near-zero setup times. These dense memories let the designer specify the number of bits in each word and select the aspect ratio for each specific register file to meet the application's need.

Novelics patented circuit technologies minimizes leakage current and active power in both the memory core and the peripheral circuits. In addition, the coolREG has been optimized to meet the performance requirements of very high speed applications such as processor cache.

The coolREG IP has been thoroughly simulated and validated in silicon to ensure the highest level of manufacturability. The MemQuest™ memory compiler has been verified and characterized to ensure the highest quality of deliverables.

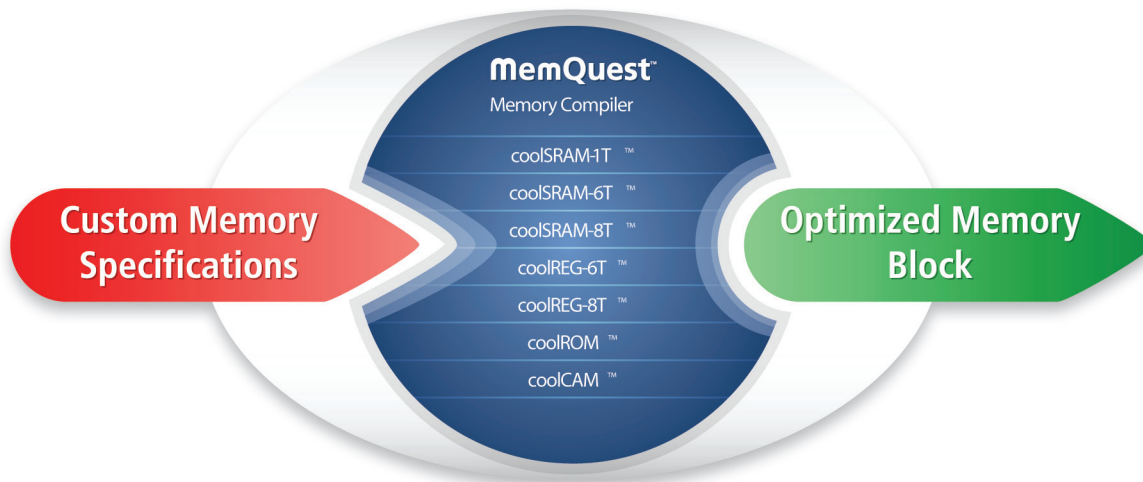
Novelics coolREG™ embedded memory IPs are ideal solutions for System-on-Chip (SoC), ASIC, and ASSP applications requiring low-power, high-speed, and high-density configurable register files. Embedded coolREG delivers the best performance and power characteristics for small and fast Register File instances.



coolREG general architecture

FEATURES:

- Customer architected through the MemQuest memory compiler and characterization tool
- Reliable, silicon-proven architecture
- Single-port, dual-port, and two-port architectures
- Based on foundry-provided 6T SRAM (single port) or 8T SRAM (dual port and two-port) cell
- Support for single and dual clock domains
- In the two-port register file, the read and write ports are completely independent and can read any location simultaneously
- The dual-port clocked register file provides two read and write ports that share the same memory space. Each port can operate in independent clock domains.
- Reliable operation and performance well beyond normal Process/Voltage/Temperature (PVT) variations
- Support for SVT & HVT Transistors
- User definable word width, depth and aspect ratio
- Memory options to meet power, speed, and area design criteria
- Easily configurable options including subword writeable
- Optimized for high performance and low-power designs
- Design utilizes up to 4 layers of metal
- Flexible routing over macro in metal 5 and above
- Supports power mesh
- Minimal setup time



MemQuest Memory Compiler Top Level Flow

Selection	Area (mm ²)	X (mm)	Y (mm)	Access Time (ns)	Power (mW)	Active Leakage (mA)	Sleep Leakage (mA)
Operating Conditions (PVT):				wc *	tc	tc	tc
1	0.822	1.29	0.635	1.4	0.003	0.337	0.0002
2	0.855	2.46	0.347	1.5	0.0045	0.341	0.0003
3	0.860	0.710	1.21	1.59	0.0024	0.341	0.0003
4	0.889	1.29	0.687	1.18	0.0025	0.343	0.0003
5	0.919	2.46	0.373	1.27	0.0033	0.344	0.0003
6	0.933	0.710	1.31	1.39	0.0022	0.353	0.0004
7	1.02	1.29	0.790	1.08	0.0024	0.357	0.0004
8	1.04	0.440	2.36	2.41	0.0031	0.355	0.0004
9	1.05	2.46	0.424	1.16	0.0029	0.352	0.0004
10	1.30	2.46	0.527	1.11	0.003	0.366	0.0005

Typical MemQuest Memory Compiler for Architectural Trade off Analysis

* Note the instance that is most optimal in each column is highlighted in green.

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