Novelics coolSRAM-1T™

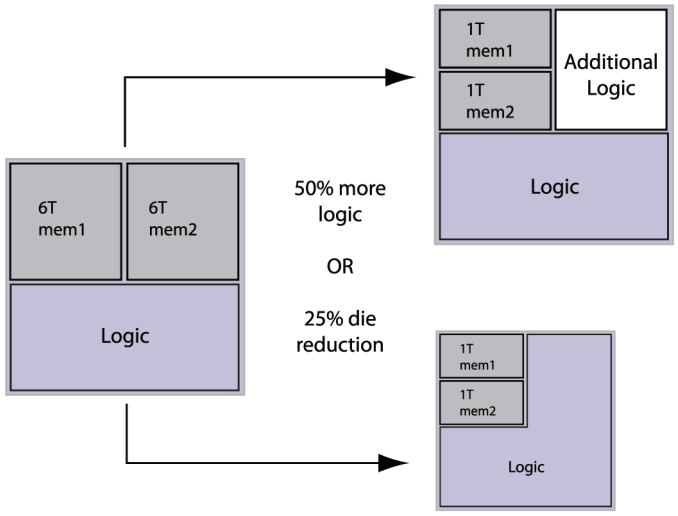
D A T A S H E E T

Novelics coolSRAM-1T embedded memory IP is the industry's only silicon-proven, single transistor SRAM IP solution that can be implemented in a bulk logic CMOS process without requiring additional masks or manufacturing steps. Use of coolSRAM-1T lowers overall system level cost and power consumption by reducing both the area of standard embedded SRAM and the number of external components.

Based on Novelics' patented SRAM-1T technology, coolSRAM-1T is an ideal solution for high density SRAM integration in ASICs, ASSPs, VLSI and System-on-Chip (SoC) applications. Embedded coolSRAM-1T blocks are custom configured by the designer and compiled to meet the design specifications, providing an unprecedented mix of low power and high density to minimize total system cost.

coolSRAM-1T IP requires only an unmodified standard logic CMOS process and therefore does not introduce additional manufacturing cost. Other single transistor SRAM offerings available on the market today require process modifications in the form of additional masks and additional manufacturing layers. These requirements can add up to 20% to the wafer cost and make other single transistor SRAM solutions not justifiable for a majority of the designs. Use of coolSRAM-1T IP even for a small amount of embedded memory can lower silicon cost significantly by reducing die size.

With the ability to reduce the die area by typically more than 25%, manufacturing yield can also be maximized. By incorporating coolSRAM-1T the design benefits from either a 50% increase in available logic area or 25% reduction in chip area for the typical SoC.



By incorporating coolSRAM-1T the design benefits from either a 50% increase in available logic area or 25% reduction in chip area.

FEATURES:

- Customer architected through the MemQuest memory compiler and characterization tool
- Circuits based on patented Novelics circuits and 1T cell design
- Standard, unmodified Logic CMOS process
- Typically twice the density of standard 6T SRAM
- Reliable operation and performance well beyond normal Process / Voltage / Temperature variations
- Higher yield than 6T due to stable circuits, smaller die area and fewer transistors
- Very low leakage current
- Supports large instances
- Bit and byte write options
- Configurable for column and/or row redundancy
- Offered in leading-edge process nodes at major foundries
- Support for SVT & HVT transistors

BENEFITS:

- Instances can be compiled with complete control of design variables
- Seamless replacement for existing SRAM-6T
- No additional mask or process layers required for manufacturing-Available as soon as the logic process is ready
- Ideal for portable applications requiring low system power and high densities
- Typical 50% increase in available logic or 25% reduction in SoC chip area over 6T- Higher density

MemQuest Memory Compiler

The Novelics MemQuest™ memory compiler is a tool unlike anything that has been available in the chip design world before. MemQuest is a WEB based on-line tool suite that enables the SoC designer to specify and implement CUSTOM memories in a matter of minutes.

Customer Memory Specifications

The chip designer begins the process by entering the specification for the memory that is needed in the design. All of the specification parameters that may drive the implementation of any memory are entered into MemQuest in pull-down menu form.

Architecture trade-off analysis

As each memory is specified, a variety of instance solutions are displayed to the designer. Each axis of performance is represented with a column in the MemQuest output table. With this table, the architecture is evaluated and the design options are traded off based on the requirements for the instance (e.g., area, power, access time, leakage current) and various operating conditions (i.e., PVT = process, voltage, and temperature). Many variables such as wider combinations of muxing and banking can be expanded. Using the MemQuest flow instances can be optimized to align exactly with their required characteristics in the chip.

Memory implementation

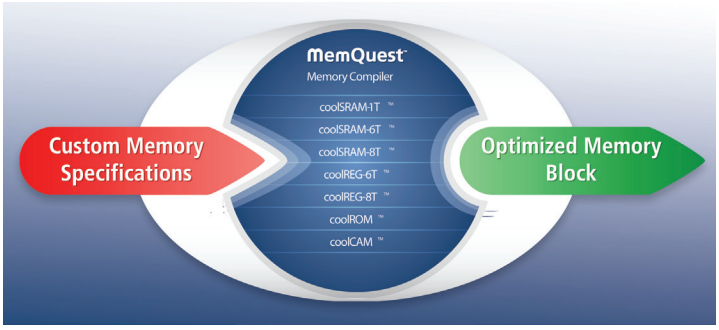
Once the specification has been completed and the architectural tradeoffs have been chosen, MemQuest immediately generates all of the views and models needed to instantiate the memory in the chip design for simulation. Additionally, the design is submitted to the Novelics on-line servers for physical implementation. A completely automated and correct by construction flow generates the physical implementation of the memory.

Memory verification

Following the automated implementation of the GDS2 for the memory instance, an additional automated program extracts the physical circuit characteristics from the GDS2 models. The program then executes a spice simulation of the exact circuit. In parallel to the automated extraction and characterization flows, another automated sequence of behind the scenes programs is run to verify the physical designs. Complete LVS and DRC verifications are run on each memory as part of this process.

Because each instance is actually characterized and verified by the on-line tools, many more degrees of freedom are available for specification by the designer who uses MemQuest. Using this flow, memories can be characterized at any number of custom corners.

Selection	Area (mm^2)	X (mm)	Y (mm)	Access Time (ns)	Power (mW)	Active Leakage (mA)	Sleep Leakage (mA)
Operating Conditions (PVT):				wc *	tc	tc	tc
1	**0.218**	0.443	0.492	6.7	0.182	0.0469	**0.0007**
2	0.220	0.856	0.257	6.39	0.288	0.0375	0.0007
3	0.227	**0.236**	0.962	7.73	0.136	0.0698	0.0009
4	0.234	1.68	**0.139**	6.38	0.507	0.034	0.0009
5	0.245	0.443	0.553	5.73	**0.129**	0.035	0.0011
6	0.246	0.856	0.287	5.39	0.183	0.0253	0.0009
7	0.260	1.68	0.154	5.37	0.296	0.0216	0.0011
8	0.298	0.856	0.348	4.91	0.13	0.0202	0.0014
9	0.311	1.68	0.185	4.87	0.191	0.0162	0.0015
10	0.413	1.68	0.246	**4.63**	0.138	**0.0151**	0.0022



MemQuest is the world's first WEB based on-line CUSTOM memory development tool suite – not merely a narrowly characterizedinstance generator.

For the latest product information, call us or visit: www.mentor.com

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004