Novelics coolSRAM-6T™

DATASHEET

Novelics' coolSRAM-6T embedded memory IP is an ideal solution for ASIC, ASSP and System-on-Chip (SoC) applications with stringent power, speed or area requirements. Embedded coolSRAM-6T is designed to deliver the best performance and power characteristics at any given instance size.

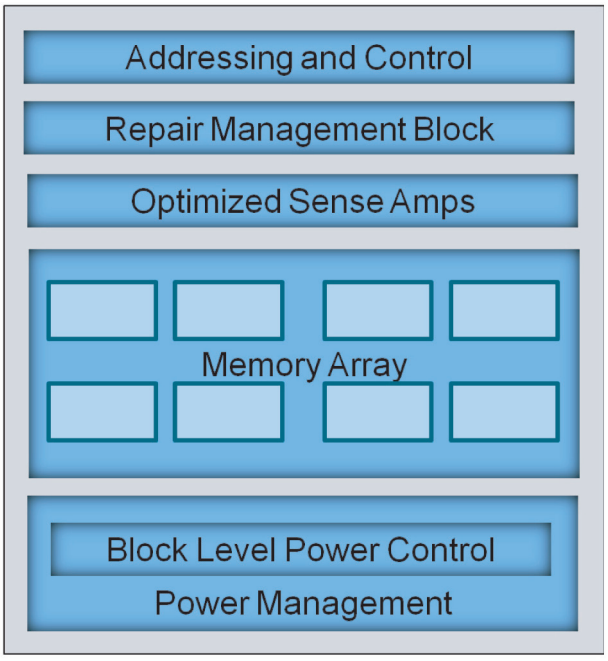
The coolSRAM-6T IP is based on the production-proven, foundry-provided 6T SRAM cell and offers advanced leakage control features, near zero setup times and optional column and row redundancy.

Use of patented Novelics circuit technologies minimize leakage current and active power in both the memory core and the peripheral circuit. This is complemented by optional power management modes that can be applied to the entire memory core or restricted to specific memory blocks. In addition, the SRAM-6T has been optimized to meet the performance requirements of very high speed applications such as processor cache.

The coolSRAM-6T IP has been thoroughly silicon validated to ensure the highest level of manufacturability. The compilers have been extensively verified and characterized to help ensure the highest quality of deliverables.

MemQuest Memory Compiler

The Novelics MemQuest™ memory compiler is a tool unlike anything that has been available in the chip design world before. MemQuest is a WEB based on-line tool suite that enables the SoC designer to specify and implement CUSTOM memories in a matter of minutes.



coolSRAM-6T general architecture

FEATURES:

- Features- Customer architected through the MemQuest memory compiler and characterization tool
- Based on foundry-provided 6T SRAM cell
- Reliable, silicon-proven architecture
- Single port architecture
- Reliable operation and performance well beyond normal Process / Voltage / Temperature variations
- Supports large instances
- Selectable power, speed, and area- Selectable word width, depth and aspect ratio
- Easily configurable options including column and/or row redundancy, subword writeable and ECC- Advanced power management sleep modes
- Block-by-block leakage power management
- Optimized for high performance and low power designs
- Uses only up to metal 4
- Supports power mesh and power ring
- Flexible routing over macro in M5 and above
- Near zero setup time
- Supports industry standard BIST and BISR methodologies
- Advance manufacturing defect detection through margin setting test modes
- Offered in leading-edge process nodes at major foundries
- Support for SVT & HVT transistors

Customer Memory Specifications

The chip designer begins the process by entering the specification for the memory that is needed in the design. All of the specification parameters that may drive the implementation of any memory are entered into MemQuest in pull-down menu form.

Architecture trade-off analysis

As each memory is specified, a variety of instance solutions are displayed to the designer. Each axis of performance is represented with a column in the MemQuest output table. With this table, the architecture is evaluated and the design options are traded off based on the requirements for the instance (e.g., area, power, access time, leakage current) and various operating conditions (i.e., PVT = process, voltage, and temperature). Many variables such as wider combinations of muxing and banking can be expanded. Using the MemQuest flow instances can be optimized to align exactly with their required characteristics in the chip.

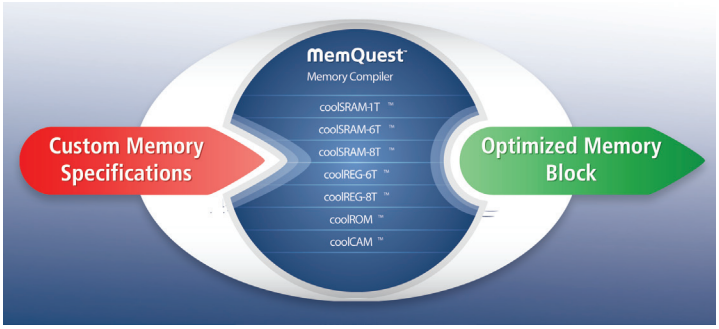
Selection	Area (mm^2)	X (mm)	Y (mm)	Access Time (ns)	Power (mW)	Active Leakage (mA)	Sleep Leakage (mA)
Operating Conditions (PVT):				wc *	tc	tc	tc
1	**0.822**	1.29	0.635	1.4	0.003	**0.337**	**0.0002**
2	0.855	2.46	**0.347**	1.5	0.0045	0.341	0.0003
3	0.860	0.710	1.21	1.59	0.0024	0.341	0.0003
4	0.889	1.29	0.687	1.18	0.0025	0.343	0.0003
5	0.919	2.46	0.373	1.27	0.0033	0.344	0.0003
6	0.933	0.710	1.31	1.39	**0.0022**	0.353	0.0004
7	1.02	1.29	0.790	**1.08**	0.0024	0.357	0.0004
8	1.04	**0.440**	2.36	2.41	0.0031	0.355	0.0004
9	1.05	2.46	0.424	1.16	0.0029	0.352	0.0004
10	1.30	2.46	0.527	1.11	0.003	0.366	0.0005

Memory implementation

Once the specification has been completed and the architectural tradeoffs have been chosen, MemQuest immediately generates all of the views and models needed to instantiate the memory in the chip design for simulation. Additionally, the design is submitted to the Novelics on-line servers for physical implementation. A completely automated and correct by construction flow generates the physical implementation of the memory.

Memory verification

Following the automated implementation of the GDS2 for the memory instance, an additional automated program extracts the physical circuit characteristics from the GDS2 models. The program then executes a spice simulation of the exact circuit. In parallel to the automated extraction and characterization flows, another automated sequence of behind the scenes programs is run to verify the physical designs. Complete LVS and DRC verifications are run on each memory as part of this process. Because each instance is actually characterized and verified by the on-line tools, many more degrees of freedom are available for specification by the designer who uses MemQuest. Using this flow, memories can be characterized at any number of custom corners.



MemQuest is the world's first WEB based on-line CUSTOM memory development tool suite – not merely a narrowly characterizedinstance generator.

For the latest product information, call us or visit: www.mentor.com

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