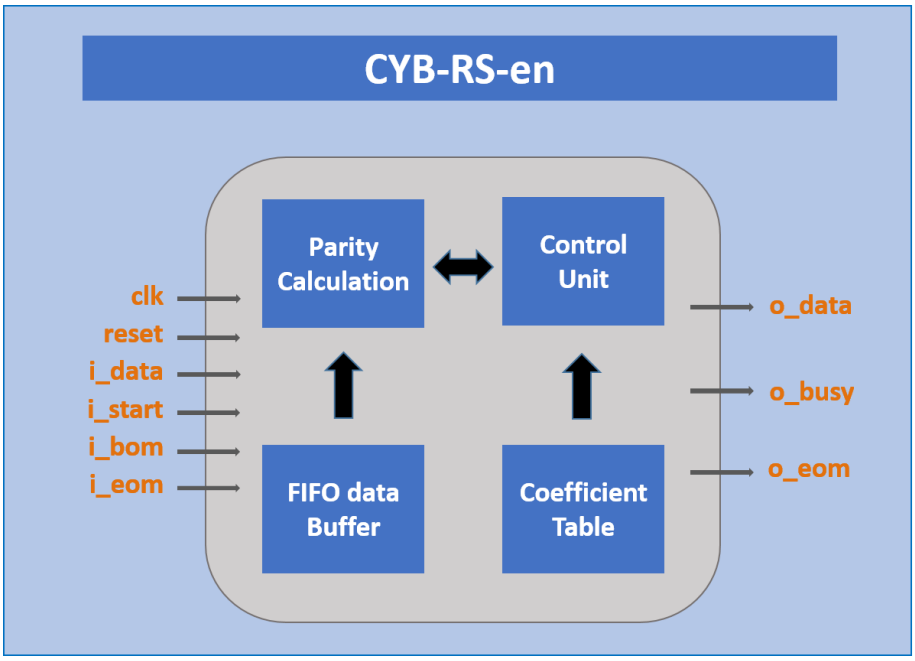
Overview of Reed Solomon Encoder IP



CYB-RS-en core implements the Reed Solomon encoding algorithm and is parameterized in terms of bits per symbol, maximum codeword length and maximum number of parity symbols. It is intended for use in a wide range of applications requiring forward error correction and can be targeted in any FPGA technologies.

Redundancy Reed-Solomon code is inserted in the transmitted information bit-stream. This redundant information is used for channel noise elimination. The error correction capability of a FEC system is strongly depended on the amount of redundancy as well as on the coding algorithm itself. The Reed-Solomon encoder accepts a K symbol information block and outputs the information block unaltered appended with 2T parity symbols, thus forming an N symbol codeword, where N=K+2T (generally called as RS(N,K) code).

Feature

- Parameterizable bits per symbol
- Programmable codeword length
- Programmable number of errors
- User configured primitive field polynomial
- User configured generator polynomial

Deliverable

- Flexible licensing
- Documentation
- Netlist
- Verilog or VHDL
- Technical support

Application

- Digital Video Broadcast (DVB)
- Digital Satellite Broadcast
- ADSL Transceivers
- Wireless Broadband Systems
- Data Storage and Retrieval Systems (e.g. CD-ROM, DVD, Compact Flash)