



## Arasan Chip Systems Announces MIPI® conformant Camera Serial Interface (CSI-3) Receiver IP Core

*Arasan's leadership in CSI-2, UniPro and M-PHY® solutions leveraged and extended to deliver IP Core for latest camera interface for mobile applications processors*

**San Jose, California – December 3, 2012** - Arasan Chip Systems, Inc. ("Arasan"), a leading provider of Total IP Solutions, announced today the addition of MIPI Alliance CSI-3 Receiver IP along with a matching Type 1 M-PHY to the company's expansive MIPI portfolio. The CSI-3 Receiver and M-PHY's can be delivered to customers in configurations of 1 to 4 receive lanes.

MIPI's CSI-3 specification is the application layer definition of the latest generation of camera serial interface that utilizes UniPro v. 1.41 as its link layer and the M-PHY v. 2.0 as the physical layer. Like CSI-2, the CSI-3 receiver is meant to deliver its image payload to an on-chip Image Signal Processor (ISP). However, when compared to CSI-2 with D-PHY, the CSI-3/UniPro/M-PHY combination provides higher bandwidth and lower power consumption per bit transferred from a camera module or bridge chip to a receiver in a mobile applications processor.

Over the past two years Arasan has made significant investment in the development and customer adoption of IP's that have direct relevance to CSI-3. For example, UFS is a JEDEC application layer standard for mobile storage which, like CSI-3, leverages UniPro and M-PHY as its lower level protocol stack. Through successful deployment of its market leading UFS solution Arasan has mastered the implementation complexities of the UniPro link layer with its software stack, and the M-PHY across multiple advanced process nodes. Over the past three years Arasan has been shipping the CSI-2 Receiver IP, which plugs into differing system and ISP bus variants. Such a rich history of product delivery has created a portfolio of mature reusable blocks which, when combined with the new CSI-3 application layer, provide customers the ability to rapidly integrate the CSI-3 receiver capability into applications processors and camera bridge chips.

"Our ability to announce our readiness to engage with CSI-3 Receiver customers within a few weeks of the MIPI Board's approval of the specs is a testament of our focus in connectivity IP's for the mobile space", said Ajay Jain, Director of Product Marketing at Arasan. "Although the CSI-3 application layers were a completely new architecture, we could leverage a considerable amount of the past work we had done for CSI-2, UniPro and M-PHY. It's a case of design reuse by us for design reuse by our customers."

Arasan offers UniPro v. 1.41 as part of the CSI-3 Receiver IP, which is deliverable in source RTL form with accompanying verification IP targeted for rapid design integration. Arasan's Type 1 M-PHY's, which are licensed separately, are designed to be compatible with the CSI-3/UniPro PHY Adapter layer, with flexibility in data bus widths across the RMMI interface.

### Availability

Arasan's MIPI CSI-3 Receiver IP Core is available immediately for licensing, including Verilog HDL of the IP Core, Verification IP, synthesis scripts, and documentation. The corresponding M-PHY IP is available as

a hard macro targeted to any process node, along with all the customer required support files and documentation.

### **About Arasan**

[Arasan Chip Systems](#) is a leading provider of Total IP Solutions for mobile storage and connectivity applications. Arasan's high-quality, silicon-proven, Total IP Solutions include digital IP cores, analog PHY interfaces, verification IP, hardware verification kits, protocol analyzers, software stacks and drivers, and optional customization services for MIPI, USB, SD, SDIO, MMC/eMMC, CF, UFS, xD and many other popular standards. Arasan's Total IP products serve system architects and chip design teams in mobile, gaming and desktop computing systems that require silicon-proven, validated IP, delivered with the ability to integrate and verify both digital, analog and software components in the shortest possible time with the lowest risk.

Unlike many other IP providers, Arasan's Total IP Solution encompasses all aspects of IP development and integration, including analog and digital cores, hardware development kits, protocol analyzers, validation IP and software stacks and drivers and optional architecture consulting and customization services. Based in San Jose, CA, USA, Arasan Chip Systems has a 16 year track record of IP and IP standards development leadership.

### **About MIPI Alliance**

MIPI Alliance is a global, collaborative organization comprised of companies that span the mobile ecosystem and are committed to defining and promoting interface specifications for mobile devices. MIPI Specifications establish standards for hardware and software interfaces which drive new technology and enable faster deployment of new features and services. For more information, visit [www.mipi.org](http://www.mipi.org).

MIPI® and M-PHY® are registered mark of MIPI Alliance, Inc.

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