Arasan Chip Systems Announces Industry First Universal Flash Storage 2.0 Total IP Solution

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Arasan Leads the Industry with up to 11.6 Gbps UFS Data Rate for Low Power Mobile Storage

San Jose, California – September 19, 2013 – Arasan Chip Systems, Inc. ("Arasan"), a leading provider of Total IP Solutions for mobile applications announced today the availability of the industry first Universal Flash Storage (UFS) 2.0 Controller IP for mobile SoC and UFS device manufacturers with a MIPI M-PHY® HS Gear 3 physical interface running at 5.8 Gbps per lane and supporting up to 2 Lanes.

Arasan's UFS 2.0 controller IP supports a maximum throughput of 5.8 Gbps with M-PHY HS-G3 single lane, or 11.6 Gbps with M-PHY HS-G3 2-lane operation, meeting the greater data transfer rates and lower power requirements of advanced mobile applications such as smartphone and tablets. "Leveraging our leadership position in deploying UFS 1.1 IP to many tier-1 SoC and memory manufacturers, we have been working with leaders in the mobile industry to provide a fully functional and validated UFS 2.0 total IP solution ahead of our competition. Arasan's total IP solution provides customers the benefits of verification IP and a ready to use, FPGA-based, Hardware Validation Platform while integrating Arasan's UFS 2.0 IP into their SoCs", said Andrew Haines, VP of Worldwide Marketing.

As an active contributor to the JEDEC® Solid State Technology Association and the MIPI® Alliance, Arasan's UFS 2.0 digital controller IP has incorporated the MIPI UniProSM version 1.6 link layer with support for multi-lane operation and the optional Unified Memory Architecture (UMA) implementation. Arasan's UFS 2.0 IP is available in both a Device Controller IP and Host Controller IP configurations, which incorporates the latest UFS Host Controller Interface (HCI) version 2.0. Arasan's MIPI M-PHY® HS-G3 IP is available in GDSII format for a variety of process technologies.

In addition, Arasan's Hardware Validation Platforms enable early validation of UFS 2.0 specification by emulating either a UFS 2.0 Host or Device systems at the interface protocol level. The Hardware Validation Platform facilitates early software application development for customer designs, production testing before the UFS 2.0 storage devices are available, and it acts as a reference platform to help root- cause any incompatibilities between the device under development and the production silicon device. Arasan provides this platform for customers who are developing UFS 2.0 based platforms which provides an accelerated full-speed validation platform for early adopters. This gives customers a method of validating silicon designs with a full-speed reference platform that strictly adheres to the UFS 2.0 protocol and provides the full suite of drivers and software stacks necessary for fast time to market.

Availability Arasan's UFS 2.0 Total IP solution is available immediately for shipment, including **UFS 2.0 Host controller**IP, **Device controller** IP, Verification IP, Linux OS based Hardware Platform with UFS 2.0 Host Controller implementation, binary Linux software stack, and all associated documentation.

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