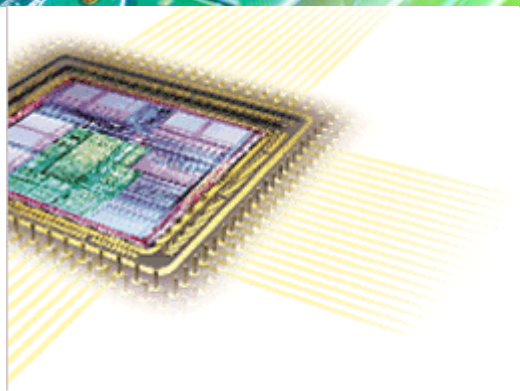
ntOFDM_BBP

OFDM Baseband Processor



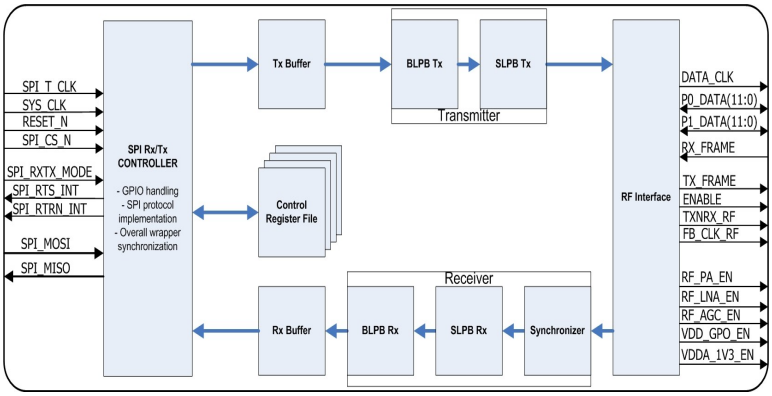
Noesis Technologies ntOFDM_BBP is a custom baseband processor, which implements the physical layer of an OFDM, time division duplexing (TDD) system. The baseband processor includes both transmission and reception bit-level and symbol-level processing chains including a sophisticated synchronization unit. The host interface is based on SPI protocol as well as with handshaking/interrupt ports. This custom system implements a subset of 802.16d standard functional options/features and is highly configurable via the integrated register-file. An RF interface module is also included, compatible with Analog Devices AD9361 RF transceiver.

The Bit-level processing block (BLPB) transmission chain implements the following functional units : randomization, FEC encoding, interleaving and symbol mapping. In BLPB reception chain the following operations are implemented: soft symbol demapping, deinterleaving, FEC decoding and de-randomization. The FEC module is based on the implementation of the Reed Solomon algorithm.

The Symbol-level processing block (SLPB) transmission chain implements the following functional units: OFDM symbol transmitter, IFFT , CP insertion. In reception chain the SLPB module is preceded by the synchronization unit, which is searching for known preamble values in order to locate the start an incoming wimax sub-frame. Once the sub-frame is located, frequency offset compensation is applied and received information is propagated down to SLPB reception chain. In SLPB reception chain the following operations take place: CP removal, FFT, OFDM symbol receiver, channel estimation, phase offset compensation and channel equalization.

Applications

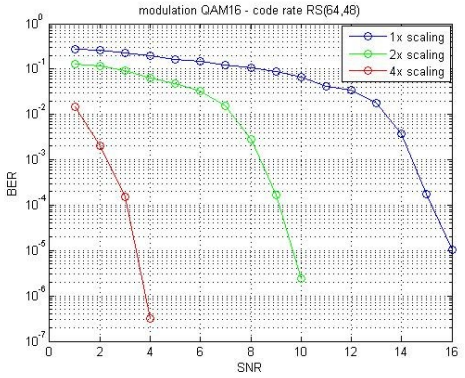
The ntOFDM_BBP core implements a custom, OFDM, TDD based baseband processor which can be used in a variety of wireless broadband applications.



Features

- Customized transmit and receive physical layer chains.
- Fully synchronous design enabling high throughput TDD operation.
- BLPB and SLPB processing blocks.
- Implements a sophisticated synchronization algorithm to efficiently detect and isolate received modulated payload information.
- Configurable as either downlink (DL) baseband station or uplink (UL) baseband station.
- Configurable data randomization, modulation level and code rate.
- Host interface based on SPI protocol.
- RF interfacing supporting Analog Devices AD9361 RF Transceiver.
- Configurable dynamic range scaling (1x, 2x or 4x) providing robust operation in channels with lower SNR value.
- Fully synchronous design.
- Silicon proven in FPGA technologies.

Performance



Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources
Altera	Cyclone IV	50140 LEs/ 299 MULT / 2 Mbits RAM

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntOFDM_BBP core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntOFDM_BBP core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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